FIG. 1A PRIOR ART

Total number of basic clocks: 62

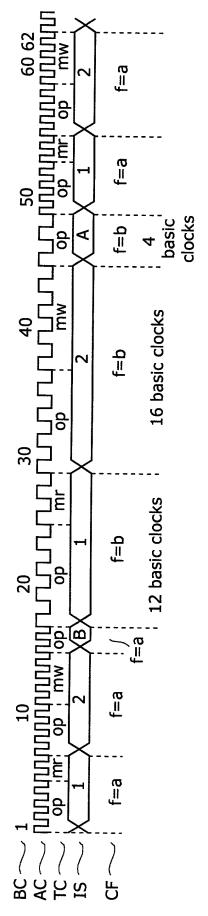


FIG. 1B

Total number of basic clocks: 52

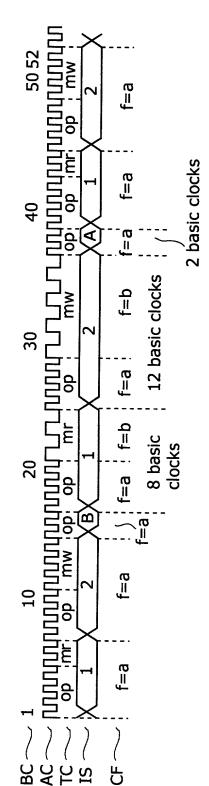


FIG. 2

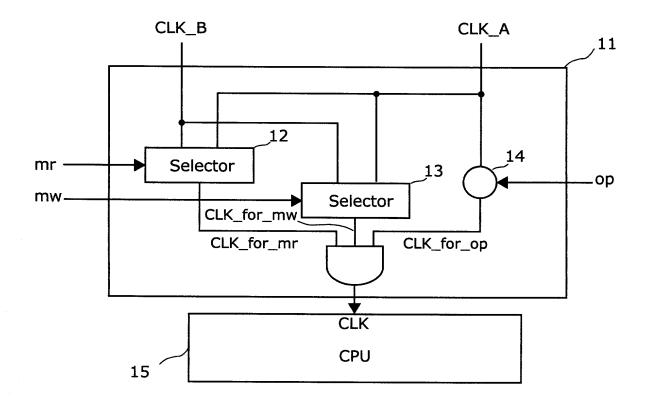


FIG. 3A

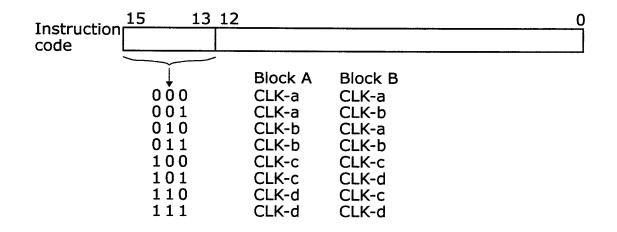


FIG. 3B

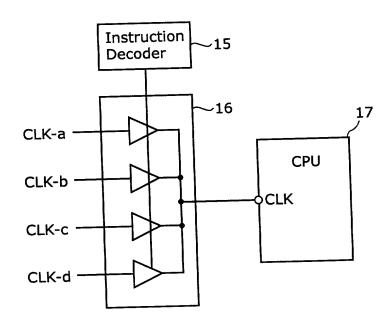


FIG. 3C

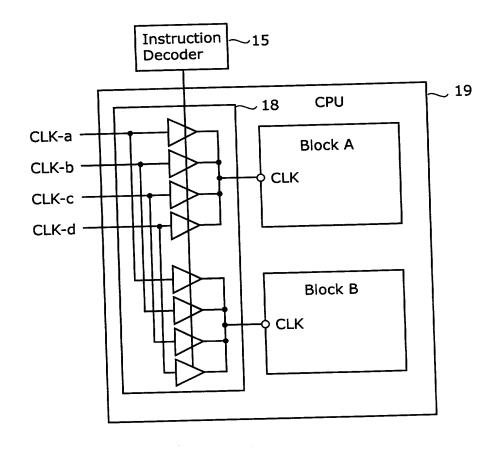
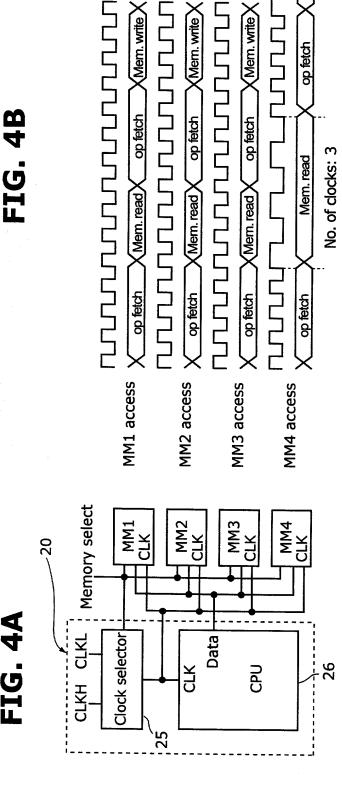


FIG. 4A



Mem. write

PRIOR ART FIG. 4C

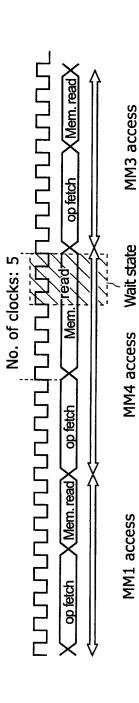


FIG. 5

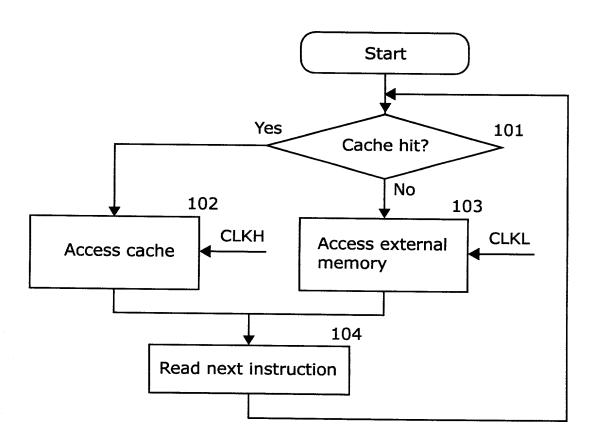


FIG. 6A PRIOR ART

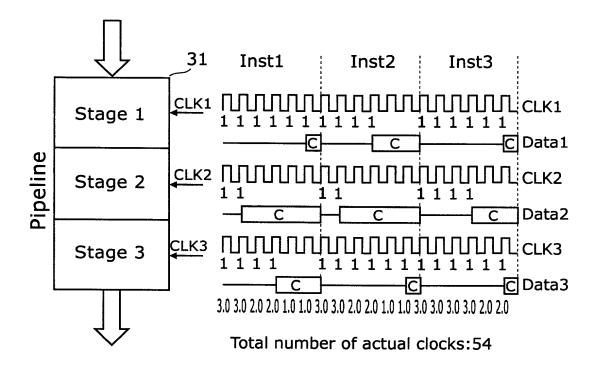


FIG. 6B

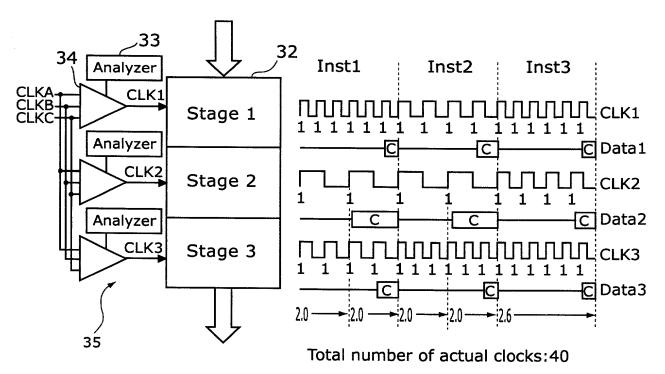


FIG. 7A

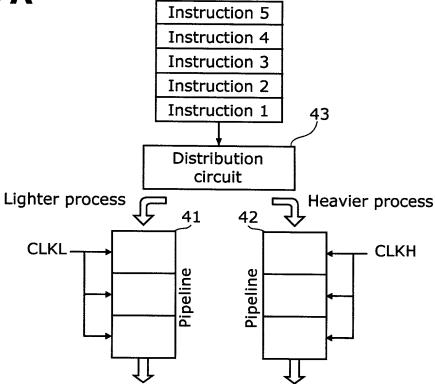


FIG. 7B

Weight of instructions

Heavier process
$$\leftarrow$$
 Lighter process a b c d e f g

FIG. 7C

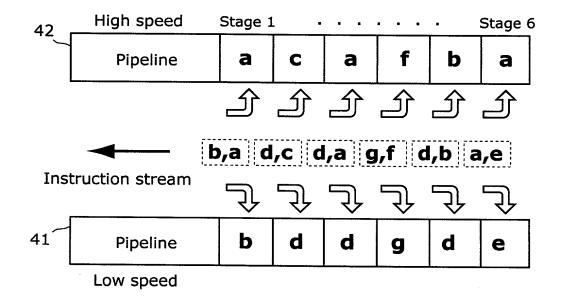
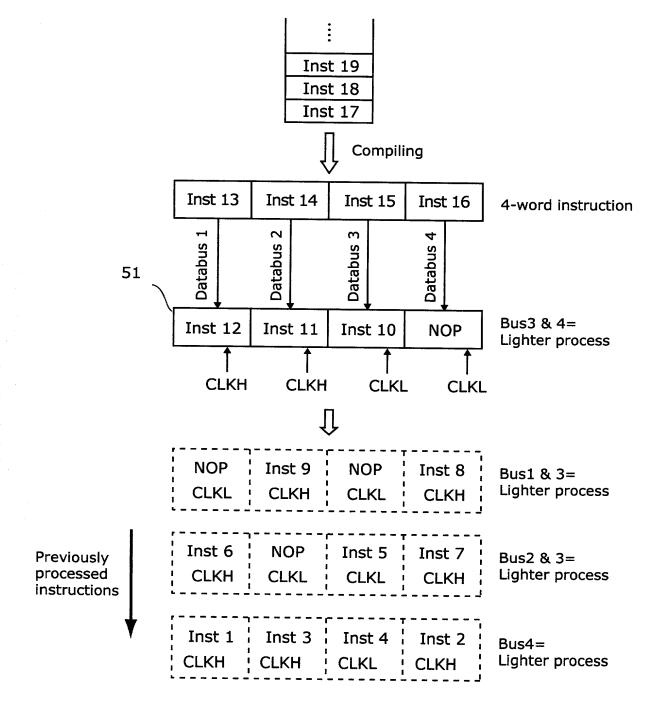


FIG. 8



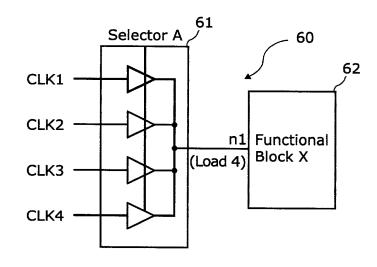


FIG. 9B

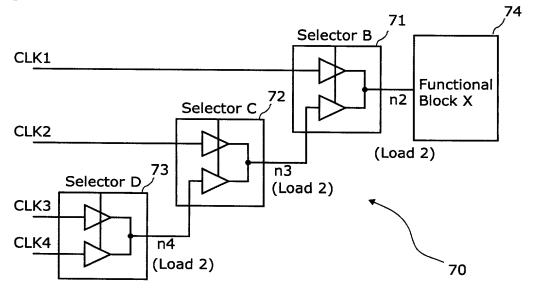


FIG. 9C

CLK Transition	CLK1	CLK2	CLK1	CLK2	CLK3
Clock selector block 60	4	4	4	4	4
Clock selector block 70	2	2	2	2	4

FIG. 10

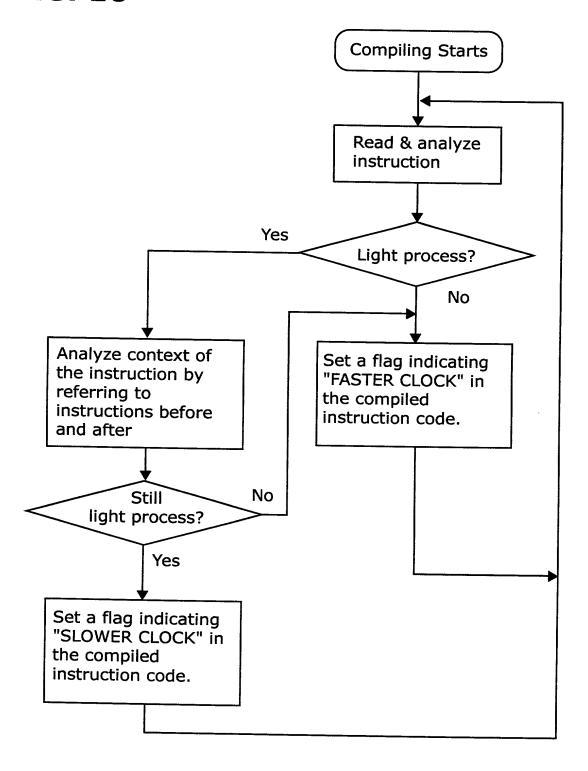


FIG. 11A PRIOR ART

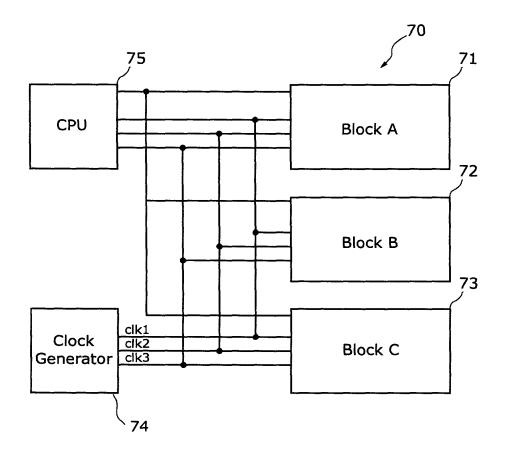


FIG. 11B PRIOR ART

Cycle	Block A	Block B	Block C
1	V		
2		V	
3	V		В
4	0	0	0
5		В	

V: Very active operation

O: Ordinally operation

B: Barely noticeable operation